IN THE CLAIMS

Please cancel Claim 16 without prejudice and without disclaimer of subject matter.

Please amend Claim 17 as shown.

1-13. (Canceled)

14. (Original) A method of forming a power MOSFET comprising the steps of:

providing a substrate of a first conductivity type;

depositing an epitaxial layer on the substrate, said epitaxial layer having a first conductivity type;

forming first and second body regions in the epitaxial layer to define a drift region therebetween, said body regions having a second conductivity type;

forming first and second source regions of the first conductivity type in the first and second body regions, respectively; and

forming a plurality of trenches in said drift region of the epitaxial layer;

epitaxially depositing in said trenches a material having a dopant of the second conductivity type, said trenches extending toward the substrate from the first and second body regions; and

diffusing at least a portion of said dopant from said trenches into portions of the epitaxial layer adjacent the trenches.

15. (Original) The method of claim 14 wherein said epitaxially deposited material filling the trench includes silicon.

16. (Canceled)

17. (Currently Amended) The method of claim ~~16~~ 14 wherein said dielectric is silicon dioxide.

18. (Original) The method of claim 14 wherein said dopant is boron.

19. (Original) The method of claim 15 further comprising the step of at least partially oxidizing said silicon

20. (Original) The method of claim 14 wherein said material filling the trench includes silicon and a dielectric.

21. (Original) The method of claim 14 wherein said body regions include deep body regions.

22. (Original) The method of claim 14, wherein said trench is formed by providing a masking layer defining at least one trench, and etching the trench defined by the masking layer.

23. (Original) The method of claim 14, wherein said body region is formed by implanting and diffusing a dopant into the substrate.

24. (Original) The method of claim 14 wherein the epitaxially depositing step includes the step of epitaxially depositing a plurality of layers, at least two of said layers having different dopant concentrations.

25. (Original) The method of claim 24 wherein said plurality of layers includes an interface layer adjacent to one of the body regions, said interface layer having a lower dopant concentration than an interior layer of the epitaxially layered material.

26. (Original) The method of claim 14 wherein said epitaxially layered material has a dopant concentration that is reduced in the vicinity of the body regions relative to the dopant concentration profile in the vicinity of the substrate.

27. (Original) The method of claim 1 wherein said portions of the epitaxial layer adjacent the trenches have a substantially uniform dopant concentration in a direction lateral to the trenches.

28. (Original) The method of claim 26 wherein said portions of the epitaxial layer adjacent the trenches have a substantially uniform dopant concentration in a direction lateral to the trenches.

29. (Original) A power MOSFET made in accordance with the method of claim 14.